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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,258	02/26/2004	Jaime Bayan	NSC1P295/P05886	9477

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,258	BAYAN ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9-13 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9-13 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The RCE and the amendment filed on 08/18/06 have being acknowledged. By this amendment, claims 1, 8 and 14-15 are cancelled; Claims 2-7, 9-19 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

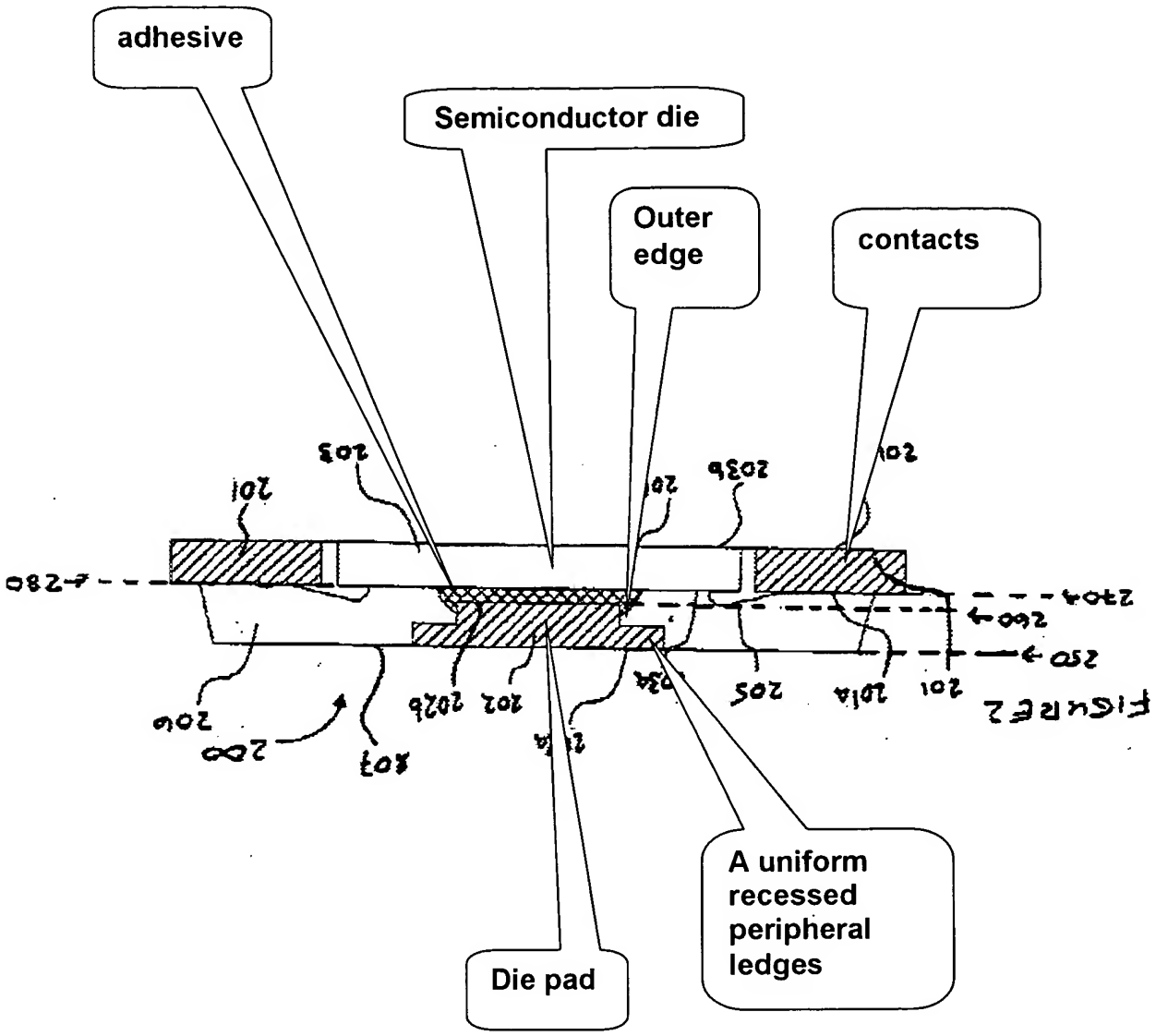
3. Claims 2-3, 5, 7, 9-10, 12 and 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Tan et al. (U.S. Pub. 2004/0124508).

Regarding claims 2 and 9, Tan in inverted Fig. 2 discloses a substrate panel for use in semiconductor packaging, the substrate panel comprising: a lead frame panel (Figs. 8-9) including a plurality of device areas, each device area having a die attach pad 202 and a plurality of contacts 201 (in inverted Fig. 2, paragraph [0033], lines 3-8), wherein each die attach pad 202 includes a die support surface 202b and a uniform peripheral ledge that is recessed relative to the die support surface, wherein the uniformly recessed peripheral ledges extend around the outer edges of the die attach pads 202 (see inverted Fig. 2 labeled by the examiner below); and

a plurality of semiconductor dies 203 (paragraph [0034], line 1), each die 203 being attached to the die support surface 202b of an associated die attach pad 202 using an adhesive 204, wherein a portion of each semiconductor die 203 extends beyond an outer edge of its associated die attach pad 202, and wherein the ledge is configured to retain an amount of the adhesive 204 (see inverted Fig. 2 labeled by the examiner below and paragraph [0034]).

Regarding claim 16, Tan in inverted Fig. 2 discloses a substrate panel for use in semiconductor packaging, the substrate panel comprising:

a lead frame panel (Figs. 8-9) including a plurality of device areas, each device area having a plurality of contacts 201 (in inverted Fig. 2, paragraph [0033], lines 3-8) arranged around a die attach pad 202, wherein each die attach pad 202 includes a die support surface 202b and a recessed ledge portion that is lower than the die support surface 202b and extends uniformly to an edge of the die attach pad 202 (see inverted Fig. 2 labeled by the examiner below).



INVERTED FIG. 2

Regarding claims 3 and 10, Tan discloses that each die attach pad 202 has a second surface 202a opposite to the die attach surface 202b, wherein the area of the die attach surface 202b is less than the area of the second surface 202a (See Fig. 2 labeled by the examiner above).

Regarding claims 5 and 12, Tan discloses further comprising an encapsulant 206 applied to the lead frame panel, wherein the second surfaces 202a of the die attach pads 202 and the bottom surfaces of the contacts 201 are exposed on an outer surface of the encapsulant 206, and wherein the peripheral ledges retain amounts of the adhesive 204 so as to prevent the adhesive from being exposed on the outer surface of the encapsulant 206 (See inverted Fig. 2 labeled by the examiner above).

Regarding claim 7, Tan (Fig. 9) discloses that the lead frame panel comprises a matrix of tie bars 843 arranged in perpendicular rows and columns that define a two dimensional array of the device areas such that adjacent device areas are separated only by the tie bars.

Regarding claim 17, Tan discloses that the peripheral recessed ledge portions extend uniformly around all of the outer edge of the die attach pads 202 (See inverted Fig. 2 labeled by the examiner above).

Regarding claim 18, Tan discloses that a plurality of semiconductor dies 203 are attached to the die support surface 202b of each die attach pad 202 using an adhesive layer 204, wherein a portion of each semiconductor die 203 extends beyond an outer edge of its associated the die attach pad 202, wherein the ledge portion is configured to retain an amount of the adhesive 204 (See inverted Fig. 2 labeled by the examiner above).

Regarding claim 19, Tan discloses that each of the semiconductor dies 203 are electrically connected with the plurality of contacts 201 arranged around the die 203 and wherein each die 203 and associated electrical connections 205 to the contacts 201 are encapsulated 206 (See inverted Fig. 2 labeled by the examiner above).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-7, 9-13 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasebe et al. (U.S. Pat. 6,713,849) in view of Tan et al. (U.S. Pub. 2004/0124508).

Regarding claims 2 and 9, Hasebe (Figs. 8 and 18) discloses a substrate panel for use in semiconductor packaging, the substrate panel comprising: a lead frame panel 40 including a plurality of device areas 41 (Fig. 8, column 10, lines 65-67 and column 11, line 1), each device area 41 having a die attach pad 4 and a plurality of contacts 7, wherein each die attach pad 4 includes a die support surface and a peripheral ledge that is defined as a peripheral portion which extends laterally from the bottom surface of the recess 20 to the tip portion 23 (See Fig. 18 labeled by the examiner below), the peripheral ledge is recessed relative to the die support surface, wherein the peripheral ledges extend around the outer edges of the die attach pads 4; and a plurality of semiconductor dies (see Fig. 8), each die 3 being attached to the die support surface of an associated die attach pad 4 using an adhesive 5 (Fig. 18 labeled by the examiner below), wherein a portion of each semiconductor die 3 extends beyond an outer edge of its associated die attach pad 4, and wherein the ledge is configured to retain an amount of the adhesive 5 (Fig. 18 labeled by the examiner below and column 12, lines 26-36).

Hasebe does not disclose a uniformly recessed peripheral ledges.

However, Tan (Figs. 2 and 10) discloses a die pad 1002 having a first face 1002a, a second face 1002b and a cut-out portion 1035 at the periphery of second face 1002b with a uniformly recessed surface 1002c (paragraph [0049], lines 3-16) in order to provide overflow space (paragraph [0049], lines 12-13). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device of Hasebe by forming the uniformly recessed peripheral

ledges, because such a forming the uniformly recessed peripheral ledges would provide overflow space, as taught by Tan (paragraph [0049], lines 3-16).

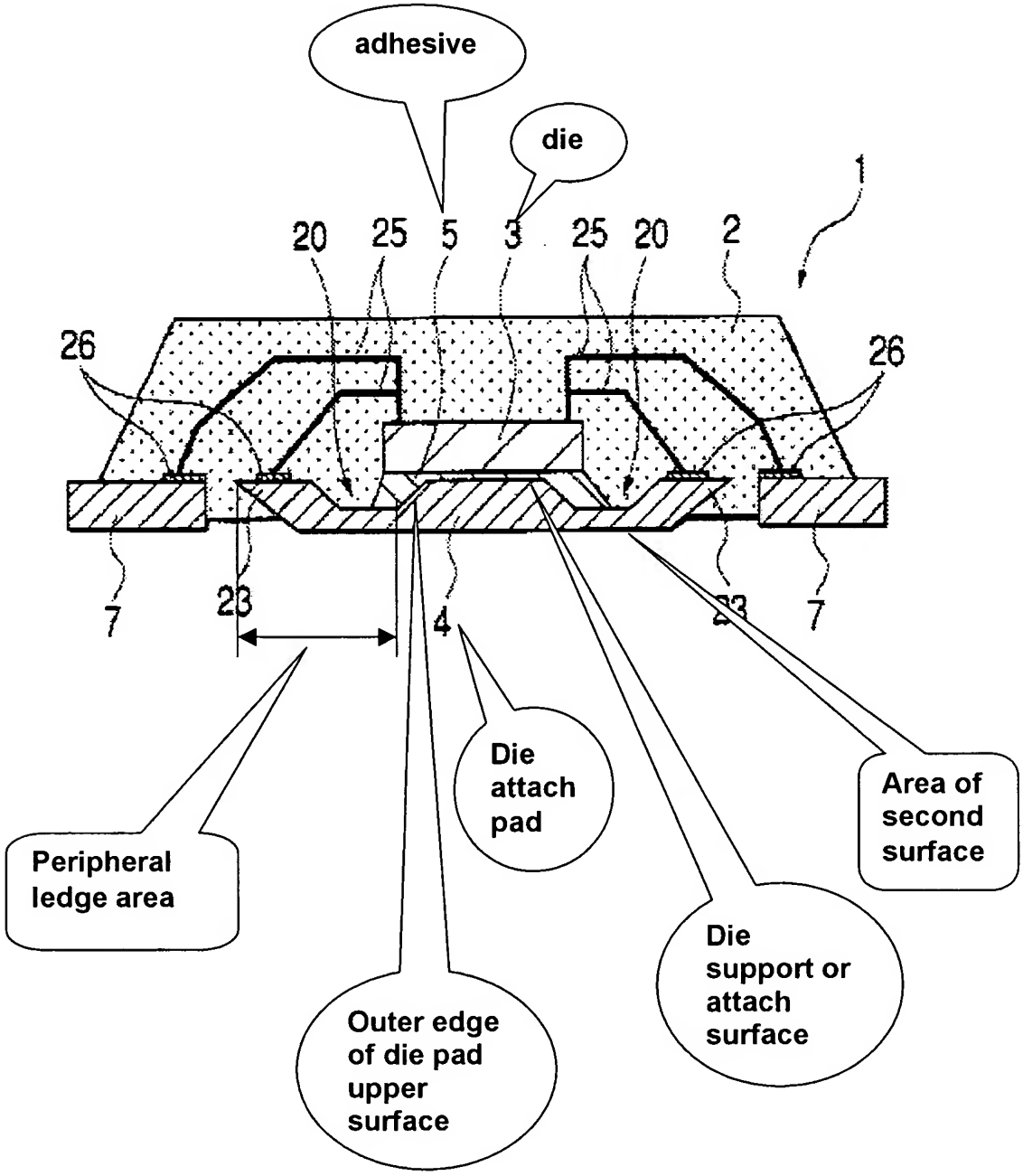
Regarding claim 16, Hasebe (Figs. 8 and 18) discloses a substrate panel for use in semiconductor packaging, the substrate panel comprising:

a lead frame panel 40 including a plurality of device areas 41 (Fig. 8, column 10, lines 65-67 and column 11, line 1), each device area 41 having a plurality of contacts arranged around a die attach pad 4, wherein each die attach pad 4 includes a die support surface and a recessed ledge that is defined as a peripheral portion which extends laterally from the bottom surface of the recess 20 to the tip portion 23 (See Fig. 18 labeled by the examiner below), the recessed ledge portion has recessed bottom surface 20 being lower than the die support surface and extends along an edge of the die attach pad 4 (also see Fig. 19).

Hasebe does not disclose a uniformly recessed peripheral ledges.

However, Tan (Figs. 2 and 10) discloses a die pad 1002 having a first face 1002a, a second face 1002b and a cut-out portion 1035 at the periphery of second face 1002b with a uniformly recessed surface 1002c (paragraph [0049], lines 3-16) in order to provide overflow space (paragraph [0049], lines 12-13). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device of Hasebe by forming the uniformly recessed peripheral ledges, because such a forming the uniformly recessed peripheral ledges would provide overflow space, as taught by Tan (paragraph [0049], lines 3-16).

FIG. 18


adhesive
die
1
20
25
5
3
25
20
2
26
26
7
23
4
23
7
Peripheral ledge area
Die attach pad
Area of second surface
Outer edge of die pad upper surface
Die support or attach surface

Regarding claims 3 and 10, Hasebe discloses that each die attach pad 4 has a second surface opposite to the die attach surface, wherein the area of the die attach surface is less than the area of the second surface (See Fig. 18 labeled by the examiner above).

Regarding claims 4 and 11, Hasebe (Fig. 18) discloses that bottom surfaces of the contacts 7 are substantially co-planar with bottom surfaces of the die attach pads 4.

Regarding claims 5 and 12, Hasebe discloses further comprising an encapsulant 2 applied to the lead frame panel 40, wherein the second surfaces of the die attach pads 4 and the bottom surfaces of the contacts 7 are exposed on an outer surface of the encapsulant 2, and wherein the peripheral ledges retain amounts of the adhesive 5 so as to prevent the adhesive from being exposed on the outer surface of the encapsulant 2 (column 12, lines 26-36).

Regarding claims 6 and 13, Hasebe discloses that the semiconductors dies 3 are down bonded to the respective ledges of their associated die attach pads 4 (Fig. 18 labeled by the examiner above).

Regarding claim 7, Hasebe discloses that the lead frame panel 40 comprises a matrix of tie bars 9 arranged in perpendicular rows and columns that define a two dimensional array of the device areas such that adjacent device areas 1 are separated only by the tie bars (Fig. 21 and column 15, lines 35-47).

Regarding claim 17, Hasebe discloses that the peripheral ledge extend entirely around the outer edge of the die attach pads (See Fig. 18 above).

Regarding claim 18, Hasebe discloses that a plurality of semiconductor dies are attached to the die support surface of each die attach pad 4 using an adhesive layer 5, wherein a portion of each semiconductor die 3 extends beyond an outer edge of its associated the die attach pad 4, wherein the ledge is configured to retain an amount of the adhesive 5 (See Fig. 18 above and column 12, lines 26-36).

Regarding claim 19, Hasebe discloses that each of the semiconductor dies 3 are electrically connected with the plurality of contacts 7 arranged around the die 3 and wherein each die 3 and associated electrical connections 25 to the contacts 7 are encapsulated by a resin 2.

Response to Arguments

6. Applicant's arguments with respect to claims 2-7, 9-19 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant argues that Hasebe fails to disclose a uniformly recessed peripheral ledges.

However, the reference of Tan is applied in the new ground of rejection to show the invention as claimed. Specifically, in Fig. 2 of Tan discloses a die attach pad 202, wherein each die attach pad 202 includes a die support surface 202b and a uniform peripheral ledge that is recessed relative to the die support surface, wherein the uniformly recessed peripheral ledges extend around the outer edges of the die attach pads 202.

The rest of applicant's arguments have been addressed to the amended claims are considered in the rejections shown above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
September 16, 2006.